EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	217	(712/235).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:03
L2	393	(712/234).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:03
L3	343	(712/219).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:03
L4	331	(711/138).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:03
L5	16	((instruction$1 adj1 queu$3) near4 (decod$3)) same ((simultaneous$3 or parallel$3) with (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:35
L6	12	mispredict$5 with (decod$3 with (instruction$1 near4 queu$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:36
L7	47	(trac$3 near4 buffer$3) with (decod$3 near4 (multiplex$4 or select$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:36
L8	39	(trace) with (decod$3) with (parallel or simultaneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:36
L9	28	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue)))	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:36
L10	2	(decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel).clm.	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:36
L11	10	(decod$3 with (instruction$1 adj1 queu$3) with parallel).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:36
L12	2	(decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:37
L13	3	((simultaneous$3 or parallel$3) with (issu$3 or push$3 or deploy$3 or send$3 or us$3) with (queue$3 and decod$3)).clm.	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:37
L14	13	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue))).clm.	US-PGPUB; USPAT	OR	OFF	2007/05/18 08:37

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L15	28	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:37
L16	9	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue)))	EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:37
L17	0	((dieffenderfer-James$) and (doing-richard$) and (stempel-brian$) and (testa-steven$) and (tsuhiya-kenichi$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:54
L18	1	((dieffenderfer-James$) and (doing-richard$) and (stempel-brian$) and (testa-steven$) and (tsuchiya-kenichi$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:54
L19	937	((dieffenderfer-James$) or (doing-richard$) or (stempel-brian$) or (testa-steven$) or\ (tsuchiya-kenichi$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:54
L20	379	((dieffenderfer-James$) or (doing-richard$) or (stempel-brian$) or (testa-steven$) or (tsuchiya-kenichi$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:54
L21	1	((dieffenderfer) and (doing) and (stempel) and (testa) and (tsuchiya)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:55
S1	320	(712/219).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:16
S2	407	(712/234).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:16
S3	212	(712/235).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:23
S4	6	decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:26
S5	6	decod$3 near4 (instruction$1 adj1 queu$3) near4 multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:27

S6	14	(decod$3 near4 (instruction$1 adj1 queu$3)) with multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:43
S7	13	(decod$3 near4 (instruction$1 adj1 queu$3)) with parallel	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:42
S8	6	(("5165025") or ("5878254") or ("5958047") or ("6065115") or ("6269439") or ("63816783") or ("6523110")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:40
S9	7	(("5165025") or ("5878254") or ("5958047") or ("6065115") or ("6269439") or ("6381678") or ("6523110")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:40
S10	6	(decod$3 with (instruction$1 adj1 queu$3)) near4 parallel	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:42
S11	0	(decod$3 with (instruction$1 adj1 queu$3)) near4 multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:43
S12	62	(decod$3 with (instruction$1 adj1 queu$3)) with instruction$1 with load$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:43
S13	25	(decod$3 near4 (instruction$1 adj1 queu$3)) with instruction$1 with load$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 15:43
S14	20	branch$3 near4 decod$3 near4 (bypass$3 or skip$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 15:50
S15	15	(branch$3 near4 decod$3 near4 stag$3) with (instruction near4 queu$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:00
S16	10	(pre?decod$3 near4 stag$3) with (instruction near4 queu$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:01
S17	335	(711/138).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:26

S18	91	(cach$3 near4 fill$3) near4 (bypass$3 or skip$4 or forward$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:33
S19	13	(cach$3 near4 fill$3) near4 (instruction$1 near4 forward$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:33
S20	217	(712/235).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:03
S21	413	(712/234).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:03
S22	333	(712/219).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:03
S23	343	(711/138).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/05/18 08:03
S24	1195	(empty or initializ$5 or start$3 or begin$5) near4 (queue$3 or buffer$3) near4 decod$4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:07
S25	12	(empty or initializ$5 or start$3 or begin$5) near4 (queue$3 or buffer$3) near4 decod$4 near4 fetch$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:12
S26	0	(invalid adj1 data) near4 (queue$3 or buffer$3) near4 decod$4 near4 fetch$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:12
S27	3	(instruction$1 adj1 queu$3) near4 (decod$3) near4 (simultaneous$3 or parallel$3) near4 (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:15
S28	4	((instruction$1 adj1 queu$3) near4 (decod$3)) with ((simultaneous$3 or parallel$3) near4 (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:17

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S29	6	((instruction$1 adj1 queu$3) near4 (decod$3)) same ((simultaneous$3 or parallel$3) near4 (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:20
S30	15	((instruction$1 adj1 queu$3) near4 (decod$3)) same ((simultaneous$3 or parallel$3) with (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:28
S31	11	mispredict$5 with (decod$3 with (instruction$1 near4 queu$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:31
S32	44	mispredict$5 same (decod$3 with (instruction$1 near4 queu$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:31
S33	2	(simultaneous$3 or parallel$3) near4 load$3 near4 (queue$3 and decod$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/12 14:41
S34	1	(simultaneous$3 or parallel$3) near4 insert$3 near4 (queue$3 and decod$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/12 14:42
S35	4	(simultaneous$3 or parallel$3) near4 (issu$3 or push$3 or deploy$3 or send$3 or us$3) near4 (queue$3 and decod$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:23
S36	15	(decod$3 near4 (instruction$1 adj1 queu$3)) with multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 14:50
S37	3	(trac$3 near4 buffer$3) near4 (decod$3 near4 (multiplex$4 or select$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 14:51
S38	47	(trac$3 near4 buffer$3) with (decod$3 near4 (multiplex$4 or select$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 14:58
S39	7	(trace near4 buffer$3) same (decod$3 near4 (multiplex$4 or select$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:01

S40	0	(trace near4 buffer$3) near4 (decod$3) near4 (parallel or simultaneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:01
S41	3	(trace near4 buffer$3) with (decod$3) with (parallel or simultaneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:03
S42	38	(trace) with (decod$3) with (parallel or simultaneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:03
S43	10	(trace) with (decod$3) with (parallel or simultaneous$2) with (load$3 or execut$3 or operat$3 or stor$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:07
S44	286	(trace) with (decod$3) with (instruction$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:07
S45	129	(trace) with (decod$3) with (instruction$1) with cach$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:07
S46	95	(trace) with (decod$3) with (instruction$1 near4 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:08
S47	93	(trace near4 (buffer$1 or memor$3 or cach$3)) with (decod$3) with (instruction$1 near4 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:08
S48	0	((simultaneous$3 or parallel$3) near4 (issu$3 or push$3 or deploy$3 or send$3 or us$3) near4 (queue$3 and decod$3)).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:25
S49	3	((simultaneous$3 or parallel$3) with (issu$3 or push$3 or deploy$3 or send$3 or us$3) with (queue$3 and decod$3)).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:25
S50	2	(decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:28
S51	10	(decod$3 with (instruction$1 adj1 queu$3) with parallel).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:28

S52	2	(decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:28
S53	10	(decod$3 with (instruction$1 adj1 queu$3) with parallel).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:29
S54	18	((load$3 or fetch$3) near4 instruction$1 near4 decoder near4 (instruction adj1 queue))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:32
S55	26	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue)))	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:34
S56	1	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue))).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:34
S57	26	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:34
S58	122	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:34
S59	9	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue)))	EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:34
S60	13	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue))).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:35

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[instruction queue" + (decoder or decoding or] Search

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All Results

D Tullsen
J Tendler
H Hirata
D Witt
H Akkary

Data processing system with instruction queue having tags indicating outstanding data status - all 2 versions »
TN Hicks, MH NguyenPhu - US Patent 5,150,470, 1992 - Google Patents
... The instruction decoding means in the preferred ... 35 embodiment includes the capability
to decode multiple many of ... are stored in an instruction queue (the memory ...
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Improving CISC instruction decoding performance using a fill unit - all 6 versions »
M Smotherman, M Franklin - Proceedings of the 28th annual international symposium on ..., 1995 - portal.acm.org
... only the first instruction in the instruction queue can produce ... triple-instruction-
decode microoperations using P6-like decoder, ... Figure 5: Fill unit decoding, ...
Cited by 29 - Related Articles - Web Search - BL Direct

An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads - all 6 versions »
H Hirata, K Kimura, S Nagamine, Y Mochizuki, A ... - Computer Architecture, 1992. Proceedings.. The 19th Annual ..., 1992 - ieeexplore.ieee.org
... So, on the average, the buffer in one instruction queue unit is filled ... A decode unit
gets an instruction from an instruc- tion queue unit and decodes it ...
Cited by 136 - Related Articles - Web Search - BL Direct

POWER4 system microarchitecture - all 14 versions »
JM Tendler, JS Dodson, JS Fields Jr, H Le, B ... - IBM Journal of Research and Development, 2002 - research.ibm.com
... are additional instructions in the instruction queue to be ... In the decode stages,
the instructions are placed ... it is known whether the load instruction resulted ...
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The approach to multiple instruction execution in the GMICRO/400processor
T Yoshida, M Matsuo, S Iwata - TRON Project Symposium, 1991. Proceedings., Eighth, 1991 - ieeexplore.ieee.org
... branch instruction, and the other instruction queue holds the ... of a memory operand,
and the precise decoding of an ... unit and the instruction decode unit operate ...
Cited by 28 - Related Articles - Web Search

Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading ... - all 51 versions »
DM Tullsen, SJ Eggers, JS Emer, HM Levy, JL Lo, RL ... - Proceedings of the 23rd annual international symposium on ..., 1996 - portal.acm.org
... bounded by the peak fetch and decode bandwidths, which ... We assume a 32-entry integer
instruction queue (which han- ... integer FP divide all other FP load (cache hit ...
Cited by 493 - Related Articles - Web Search - BL Direct

Apparatus for a multi-data store or load instruction for transferring multiple contiguous storage ... - all 3 versions »
T Yoshida - US Patent 5,390,307, 1995 - Google Patents
... FOR A MULTI-DATA STORE OR LOAD INSTRUCTION FOR ... in the case where aninstruc -tion
decoder has decoded ... multi-data transfer (storing or loading) instruction, bits ...
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Improved pipelined processor with two stage decoder for exchanging register values for similar ... - all 2 versions »
F Itomitsu, T Yoshida - US Patent 4,945,511, 1990 - Google Patents
... IMPROVED PIPELINEDPROCESSOR WITH TWO STAGE DECODER FOR EXCHANGING ... The D stage 72
decodes the instruction code ... IF stage 71 and outputs the decoding result to 30 ...
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Multi-instruction stream branch processing mechanism - all 3 versions »
JF Hughes, JS Liptay, JW Rymarczyk, SE Stone - US Patent 4,200,927, 1980 - Google Patents
... OR OR F IG.8 BRANC H RESULT DECODE BR · GUESS WRONG ... RESET 00,1,2,3 185 TURN OFF AB
C DECODING POINTER 189- 188- 160' I- FETCH SEQUENCER K 186 PER POINTER ...
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Multiple instruction issue in the NonStop cyclone processor - all 3 versions »
RW Horst, RL Harris, RL Jardine - ACM SIGARCH Computer Architecture News, 1990 - portal.acm.org
... instruc- tions in preparation for decoding and execution. ... mechanism, to allow it
to decode branch in ... the instruction cache into the instruction queue, and then ...
Cited by 34 - Related Articles - Web Search

[instruction queue" + (decoder or de] Search

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All Results

D Tullsen

J Lo

J Emer

S Eggers

H Levy

An Elementary Processor Architecture with **Simultaneous** Instruction Issuing from Multiple Threads - all 6 versions »
H Hirata, K Kimura, S Nagamine, Y Mochizuki, A ... - Computer Architecture, 1992. Proceedings., The 19th Annual ..., 1992 - ieeexplore.ieee.org
... So, on the average, the buffer in one **instruction queue** unit is filled ... A **decode** unit
gets an instruction from an instruc- tion queue unit and **decodes** it ...
Cited by 136 - Related Articles - Web Search - BL Direct

Exploiting choice: instruction **fetch** and issue on an implementable **simultaneous** multithreading ... - all 51 versions »
DM Tullsen, SJ Eggers, JS Emer, HM Levy, JL Lo, RL ... - Proceedings of the 23rd annual international symposium on ..., 1996 - portal.acm.org
... bounded by the peak **fetch** and **decode** bandwidths, which ... We assume a 32-entry integer
Instruction queue (which han- ... integer FP divide all other FP **load** (cache hit ...
Cited by 493 - Related Articles - Web Search - BL Direct

Improving CISC instruction **decoding** performance using a fill unit - all 6 versions »
M Smotherman, M Franklin - Proceedings of the 28th annual international symposium on ..., 1995 - portal.acm.org
... only the first instruction in the **instruction queue** can produce ... triple-instruction-
decode microoperations using P6-like **decoder**, ... Figure 5: Fill unit **decoding**, ...
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Handling long-latency **loads** in a **simultaneous** multithreading processor - all 14 versions »
DM Tullsen, JA Brown - 34th International Symposium on Microarchitecture, 2001 - doi.ieeecomputersociety.org
... operation are renaming regis- ters and **fetch/decode** bandwidth ... resource is exhausted,
such as **instruction queue** entries or ... measures to solve the long-**load** problem ...
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Circuit Implementation of a 600 MHz Superscalar RISC Microprocessor - all 17 versions »
M Matson, D Bailey, S Bell, L Biro, S Butler, J ... - International Conference on Computer Design, 1998 - doi.ieeecomputersociety.org
... block has a dedicated **decode** logic block. ... was decoded, or separate, **parallel decoders**
that examined ... from the processor's floating point **instruction queue**. ...
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Multiple instruction issue in the NonStop cyclone processor - all 3 versions »
RW Horst, RL Harris, RL Jardine - ACM SIGARCH Computer Architecture News, 1990 - portal.acm.org
... instruc- tions in preparation for **decoding** and execution. ... mechanism, to allow it
to **decode** branch in ... the instruction cache into the **instruction queue**, and then ...
Cited by 34 - Related Articles - Web Search

Deferred store data read with simple anti-dependency pipeline inter-lock control in superscalar ... - all 3 versions »
H Park, SP Song... - US Patent 5,881,307, 1999 - Google Patents
... an alternative embodiment of the invention, **decoder** 122 solely ... **Decoders** 120 and 122
extract register numbers and ... latches 124 and 126 when **decoding** instructions ...
Cited by 7 - Related Articles - Web Search

Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction ... - all 6 versions »
JG Favor, K Van Dyke, DR Stiles... - US Patent 5,649,137, 1997 - Google Patents
... mentioned abom In an aggressive **Instruction Queue** and Branch ... with the **fetching**
and/or **decoding** of a branch ... An Instruction **Decoder** (DEC) 12 performs instruction ...
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Superscalar microprocessor including flag operand renaming and forwarding apparatus - all 6 versions »
SA White, DS Christie, MD Goddard... - US Patent 5,632,023, 1997 - Google Patents
... 1991, pp. 13-18. 1992 entitled "Instruction **Decoder** and Superscalar Procès- ... FIG.
4 POPS TO BE ALLOCATED FROM **DECODE** DEPENDENCY CHECKING LOGIC ...
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Dynamic **Fetch** Engine for **Simultaneous** Multithreaded Processors - all 4 versions »
TR Yang, JJ Shieh - LECTURE NOTES IN COMPUTER SCIENCE, 2004 - Springer
... After **decoding**, the register renaming logic re- moves ... either increasing the size
of **Instruction queue** or good ... instructions it has in the **decode** unit, register ...
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[instruction queue" + (decoder or de]   Search

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